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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/666,456	09/21/2000	Takashi Miyamori	197529US2	1484

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EXAMINER	
PHAM, THOMAS K	

ART UNIT	PAPER NUMBER
2121	10

DATE MAILED: 02/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/666,456	MIYAMORI, TAKASHI	
	Examiner	Art Unit	
	Thomas K Pham	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1-9 and 11-19* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6 and 9*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Response to Amendment

1. This action is in response to request for re-consideration filed on 112/2003

2. New claim 20 filed by the applicant has been entered.

3. Claims 1-9 and 11-19 has been considered but moot in view of new ground(s) of rejection.

4. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claim 20 is allowed.

DETAILED ACTION

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-9 and 11-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. U.S. Patent no. 6,018,796 (hereinafter Suzuki) in view of Purasenjitsuto et al. Japan Patent no. 09-212359 (hereinafter Purasenjitsuto)

Regarding claim 1

Suzuki teaches a processor, comprising: a processor core for executing an instruction in a pipeline processing (col. 2 lines 46-48, "The data processor ... instruction in pipeline stages"); a

data memory accessed by said processor core (col. 5 lines 33-38, "In the data processor ... by the first processing unit"); and an extended arithmetic unit (fig. 5, element 2), connected to an exterior of said processor core, for processing an extended instruction decoded in said processor core in the pipeline processing (col. 9 lines 1-8, "The instruction decoding ... into the register set 131"), said extended arithmetic unit executing an arithmetic operation by using arithmetic operation data retained in a register file in said processor core, and outputting a result of an arithmetic operation directly to a memory stage processing in said processor core (col. 12 lines 41-64, "In the case where ... data processor in MEM stage"), said processor core receiving the result of the arithmetic operation executed by said extended arithmetic unit and inputted therefrom into said register file in said processor core (col. 9 lines 9-17, "This instruction execution ... writes the data into the register set 131 via the buffer 138c") but does not teach the processor core includes a pipeline controller for flushing or stopping the pipeline processing in said extended arithmetic unit. However, Purasenjitsuto teaches the technique to stop execution of the extended operation unit by outputting pipeline stop signal to the extended unit connected to inside processor (paragraphs 51, 59 and 61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the pipeline stopping signal of Purasenjitsuto with the processor of Suzuki because it would provide for controlling stalling or stopping effect to the pipelines in order to attain synchronization within the processor.

Regarding claim 2

Suzuki teaches

A processor, comprising: a processor core for executing an instruction in a pipeline processing (col. 2 lines 46-48, "The data processor ... instruction in pipeline stages"); a data memory

accessed by said processor core (col. 5 lines 33-38, "In the data processor ... by the first processing unit"); and an extended arithmetic unit, connected to an exterior of said processor core, for processing an extended instruction decoded in said processor core in the pipeline processing (col. 9 lines 1-8, "The instruction decoding ... into the register set 131"), said processor core, at least including an instruction memory for storing an instruction to be executed (col. 4 lines 60-63, "The data processor ... perform pipeline processing"); an instruction decode unit for reading out an instruction from said instruction memory to decode the instruction (col. 6 lines 54-58, "The instruction decoding ... the pipeline stages"), in case that the instruction decoded is an extended instruction that should be executed by said extended arithmetic unit connected to the exterior of said processor core, said instruction decode unit also outputting at least an instruction code of said extended instruction to said extended arithmetic unit (col. 9 lines 1-8, "The instruction decoding ... into the register set 131"); a register file for retaining arithmetic operation data of an arithmetic operation that should be executed by the instruction decoded, in case that said arithmetic operation data is data of said extended instruction, said register file also outputting said arithmetic operation data to said extended arithmetic unit (col. 9 lines 9-17, "This instruction execution ... writes the data into the register set 131 via the buffer 138c"); a first operational section for executing the instruction decoded (col. 9 lines 1-8, "The instruction decoding ... into the register set 131"); an extended arithmetic unit, at least including, a second operational section for executing an arithmetic operation specified by said extended instruction by using said arithmetic operation data retained in said register file (col. 9 lines 43-54, "The extended instruction ... processing is selectively controlled"), and outputting an execution result of the arithmetic operation directly to a memory stage processing in said

processor core (col. 12 lines 41-64, "In the case where ... data processor in MEM stage"). However, Purasenjitsuto teaches the technique to stop execution of the extended operation unit by outputting pipeline stop signal to the extended unit connected to inside processor (paragraphs 51, 59 and 61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the pipeline stopping signal of Purasenjitsuto with the processor of Suzuki because it would provide for controlling stalling or stopping effect to the pipelines in order to attain synchronization within the processor.

Regarding claims 3 and 13

Suzuki teaches in case that the instruction decoded is said extended instruction, said processor core outputs to said extended arithmetic unit at least an instruction code that specifies an action involved in an arithmetic operation in said extended arithmetic unit and an instruction valid signal that indicates said instruction code is valid (col. 9 lines 43-54, "The extended instruction decoding ... processing is selectively controlled").

Regarding claims 4 and 14

Suzuki teaches the arithmetic operation data outputted to said extended arithmetic unit is a value read out from said register file in said processor core in accordance with a register number specified by a part of said extended instruction (col. 9 lines 11-16, "The instruction execution circuit 33 ... to the extended processor 2").

Regarding claims 5 and 15

Suzuki teaches the pipeline controller controls pipeline processing in an interior of said processor core and in said extended arithmetic unit (col. 13 lines 52-53, "The pipeline control circuit 192 ... register set 131 in WB stage").

Regarding claims 6 and 16

Purasenjitsuto teaches pipeline controller outputs to said extended arithmetic unit a first pipeline stop signal for stopping the pipeline processing in said extended arithmetic unit (paragraphs 51, 59 and 61).

Regarding claims 7 and 17

Purasenjitsuto teaches the pipeline controller in case that the instruction decoded is a jump instruction, outputs to said extended arithmetic unit a pipeline flush signal for flushing a register in said extended arithmetic unit (paragraph 47).

Regarding claims 8 and 18

Purasenjitsuto teaches the extended arithmetic unit further comprises a second pipeline controller for, in case that the extended instruction requires more than one cycle asserting a second pipeline stop signal for stopping the pipeline processing in said processor core (paragraph 39)

Regarding claims 9 and 19

Suzuki teaches teaches extended arithmetic unit outputs to said processor core an arithmetic operation result invalidating signal that invalidates an execution result of an arithmetic operation executed in said processor core (col. 15 lines 10-17, "the operation result ... through the selector 97").

Regarding claim 11

Suzuki teaches the extended arithmetic unit includes: a plurality of pipeline-structured arithmetic circuits (fig. 9); a first pipeline register for storing a processing result by an arithmetic circuit in a preceding stage at a rising of a following clock (col. 15 lines 37-44, "In the case of an extended ... by the latch 234"); and a second pipeline register for storing a processing result by an

arithmetic circuit in a succeeding stage at the rising of the following clock (col. 15 lines 58-63, "the operation result ... in the data processor 4").

Regarding claim 12

Suzuki teaches a processor core, connected to an extended arithmetic unit for processing an extended instruction decoded in said processor core in pipeline processing and for executing an instruction, in a pipeline processing, comprising: an instruction memory for storing an instruction to be executed (col. 5 lines 33-38, "In the data processor ... by the first processing unit"); an instruction decode unit for reading out an instruction from said instruction memory to decode the instruction, in case that the instruction decoded is an extended instruction that should be executed by said arithmetic unit connected to the exterior of said processor core, said instruction decode unit also outputting at least an instruction code of said extended instruction to said extended arithmetic unit (col. 9 lines 1-8, "The instruction decoding ... into the register set 131"); and a register file for retaining arithmetic operation data of an arithmetic operation that should be executed by the instruction decoded, and in case that said arithmetic operation data is data for said extended instruction, said register file also outputting said arithmetic operation data to said extended arithmetic unit (col. 9 lines 9-17, "This instruction execution ... writes the data into the register set 131 via the buffer 138c"), storing a result of an arithmetic operation executed in said extended arithmetic unit, and outputted directly to a memory stage processing in said processor core (col. 12 lines 41-64, "In the case where ... data processor in MEM stage"); a first operational section for executing the instruction decoded (col. 9 lines 1-8, "The instruction decoding ... into the register set 131") but does not teach a pipeline controller for flushing or stopping the pipeline processing in said extended arithmetic unit. However, Purasenjitsuto

teaches the technique to stop execution of the extended operation unit by outputting pipeline stop signal to the extended unit connected to inside processor (paragraphs 51, 59 and 61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the pipeline stopping signal of Purasenjitsuto with the processor of Suzuki because it would provide for controlling stalling or stopping effect to the pipelines in order to attain synchronization within the processor.

Response to Arguments

In the remark the applicant argues that cited reference fails to disclose:

I) "flushing or stopping the pipeline processing in said extended arithmetic unit" as to claims 1, 2 and 12.

In response to applicant's argument,

I) It is noted that prior art (Purasenjitsuto et al. Japan Patent no. 09-212359) teaches (paragraphs 51, 59 and 61) and (fig. 7 and 10) technique to stop execution of the extended operation unit tentatively by outputting pipeline stop signal to the extended operation unit connected inside processor. Therefore, the limitations are met by the combination of the references.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thomas Pham*; whose telephone number is (703) 305-7587 and fax number is (703) 746-8874, Monday-Thursday and every other Friday from 7:30AM- 5:00PM EST or contact Supervisor *Mr. Anil Khatri* at *(703) 305-0282.*

Any response to this office action should be mailed to: **Director of Patents and Trademarks Washington, D.C. 20231**, or **Hand-delivered** responses should be brought to **Crystal Park II, 2121 Crystal Drive Arlington, Virginia, (Receptionist located on the 4th floor),** or fax to the **official fax number (703) 872- 9306.**

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Thomas Pham
Patent Examiner

TP

January 28, 2004

ANIL KHATRI
SUPERVISORY PATENT EXAMINER